## APPENDIX A

Please cancel claims 95 - 97, 103, 104, 174 - 186, 282, 283, 286 - 300, and 302 - 379.

Please amend claims 98 - 102, 105 - 173, 187 - 281, 284, and 285, as follows:

98. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

an image communication link coupled to the resolution reduction circuit, the image communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

a vector communication link coupled to the subpixel vector change circuit, the vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit;

a display circuit coupled to the resolution reduction circuit, the display circuit generating display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

a display device coupled to the display circuit, the display device displaying an image in response to the display image information generated by the display circuit.

99. (Amended) A system as set forth in claim 98,

wherein the first memory is a first intermediate memory storing the prior pixel image information as intermediate prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second intermediate memory storing the next pixel image information as intermediate next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a two dimensional spatial interpolation circuit generating the spatial interpolation information as two dimensional spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the transform processor is a frequency domain transform processor generating the transformed image information as frequency domain transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a shaded weight circuit generating the weight information as shaded weight information;

wherein the scale factor circuit is a geometric scale factor circuit generating the scale factor information as geometric scale factor information;

wherein the weighting and scaling circuit is a sum of the products weighting and scaling circuit generating the scaled weighted image information as sum of the products scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a fraction removal resolution reduction circuit generating the reduced resolution image information as fraction removal reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a digital image communication link communicating the output image information as digital output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a digital vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit as digital output subpixel vector information;

wherein the display circuit is a data decompression display circuit generating the display image information as data decompression display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a CRT display device displaying the image as a CRT image in response to the display image information generated by the display circuit.

100. (Amended) A system as set forth in claim 98,

wherein the first memory is a first mosaic memory storing the prior pixel image information as prior pixel mosaic image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second mosaic memory storing the next pixel image information as next pixel mosaic image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a half pixel resolution spatial interpolation circuit generating the spatial interpolation information as half pixel resolution spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the subpixel vector change circuit is an XIP, YIP subpixel vector change circuit generating the subpixel vector change information having subpixel resolution as XIP, YIP vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the transform processor is a coordinate transform processor generating the transformed image information as coordinate transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a weight memory circuit generating the weight information as stored weight information;

wherein the scale factor circuit is a scale factor memory circuit generating the scale factor information as stored scale factor information;

wherein the weighting and scaling circuit is an antialiasing weighting and scaling circuit generating the scaled weighted image information as antialiasing scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a truncation resolution reduction circuit generating the reduced resolution image information as truncated reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a television image communication link communicating the output image information as television output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a television vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit as television output subpixel vector information;

wherein the display circuit is a composite display circuit generating the display image information as composite display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a liquid crystal display device displaying the image as a liquid crystal image in response to the display image information generated by the display circuit.

101. (Amended) A system as set forth in claim 98,

wherein the first memory is a first data base memory storing the prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second data base memory storing the next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is an antialiasing spatial interpolation circuit generating the spatial interpolation information as antialiasing spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the subpixel vector change circuit is an initial point subpixel vector change circuit generating the subpixel vector change information having subpixel resolution as initial point vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the transform processor is a Fourier transform processor generating the transformed image information as Fourier transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a subpixel coordinate weight circuit generating the weight information as subpixel coordinate weight information;

wherein the scale factor circuit is a weight scale factor circuit generating the scale factor information as weight scale factor information;

wherein the weighting and scaling circuit is a geometric weighting and scaling circuit generating the scaled weighted image information as geometric scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a roundoff resolution reduction circuit generating the reduced resolution image information as rounded off reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a data compressed image communication link communicating the output image information as data compressed output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a data compressed vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit as data compressed output subpixel vector information;

wherein the display circuit is an NTSC display circuit generating the display image information as NTSC display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a CRT display device displaying the image as a CRT image in response to the display image information generated by the display circuit.

102. (Amended) A system as set forth in claim 98,

wherein the first memory is a first image memory storing the prior pixel image information as eight bit prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second image memory storing the next pixel image information as eight bit next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a subpixel resolution spatial interpolation circuit generating the spatial interpolation information as subpixel resolution spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the subpixel vector change circuit is an initial condition subpixel vector change circuit generating the subpixel vector change information having subpixel resolution as initial condition vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the transform processor is a geometric transform processor generating the transformed image information as geometric transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a kernel weight circuit generating the weight information as kernel weight information;

wherein the scale factor circuit is a kernel scale factor circuit generating the scale factor information as kernel scale factor information;

wherein the weighting and scaling circuit is a kernel weighting and scaling circuit generating the scaled weighted image information as kernel scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is an integer resolution reduction circuit generating the reduced resolution image information as integer reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a video image communication link communicating the output image information as video output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a video vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit as video output subpixel vector information;

wherein the display circuit is a red, green, blue display circuit generating the display image information as red, green, blue display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a red, green, blue display device displaying the image as a red, green, blue image in response to the display image information generated by the display circuit.

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105. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a [spatial] temporal interpolation circuit [coupled to the first memory and coupled to the second memory, the spatial interpolation circuit] generating [spatial] temporally interpolated [interpolation] information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a subpixel vector change circuit [coupled to the first memory and coupled to the second memory, the subpixel vector change circuit] generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory; and

a transform processor [coupled to the spatial interpolation circuit, the transform processor] generating transformed image information in response to [spatial interpolation] the temporally interpolated information [generated by the spatial interpolation circuit].

106. (Amended) A system as set forth in claim 105, further comprising:

a communication link [coupled to the transform processor, the communication link] communicating output image information in response to the transformed image information [generated by the transform processor].

107. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation [circuit] processor coupled to the first memory and coupled to the second memory, the spatial interpolation [circuit] processor generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory; [and]

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a weight input circuit generating weight input information;

a weight memory;

a writing circuit coupled to the weight input circuit and coupled to the weight memory, the writing circuit writing weight information into the weight memory in response to the weight input information generated by the weight input circuit; and

a weighting processor coupled to the spatial interpolation processor and coupled to the weight memory, the weighting processor generating weighted image information in response to the spatial interpolation information generated by the spatial interpolation processor and in response to the weight information stored in the weight memory.

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108. (Amended) A system as set forth in claim 107, further comprising:

a communication link coupled to the spatial interpolation [circuit] processor, the communication link communicating output image information in response to the spatial interpolation information generated by the spatial interpolation [circuit] processor.

109. (Amended) A [system] process comprising the acts of:

[a first memory] storing a prior 64-pixel block of [pixel] image information in a first memory, the prior 64-pixel block of [pixel] image information representing a prior image;

[a second memory] storing a next 64-pixel block of [pixel] image information in a second memory, the next 64-pixel block of [pixel] image information representing a next image; [and]

generating temporally interpolated image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information; and

[a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit] generating subpixel vector change information having subpixel resolution in response to the prior 64-pixel block of image information stored [by] in the first memory and in response to the next 64-pixel block of image information stored [by] in the second memory.

110. (Amended) A [system] process as set forth in claim 109, further comprising the act of:

[a communication link coupled to the first memory and coupled to the second memory, the communication link] communicating output image information in response to the prior 64-pixel block of image information stored [by] in the first memory and in response to the next 64-pixel block of image information stored [by] in the second memory.

111. (Amended) A [system] process as set forth in claim 109, further comprising the act of [:]

[a communication link coupled to the subpixel vector change circuit and communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit] making a product.

112. (Amended) A [system] process as set forth in claim 109, further comprising the acts of:

[a display circuit coupled to the first memory and coupled to the second memory and generating display image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

a display device coupled to the display circuit and displaying an image in response to the display image information generated by the display circuit]

storing at least two digital bits of information in a plurality of levels in each of a plurality of multilevel memory cells;

generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

generating the subpixel vector change information in response to the accessed digital information.

113. (Amended) A [system] process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

[a subpixel vector change circuit] generating subpixel [vector] change information having subpixel resolution by subtracting in between the [in response to] prior pixel image information [, the prior pixel image information representing a prior image,] and [in response to] the next pixel image information [, the next pixel image information representing a next image].

114. (Amended) A [system] process as set forth in claim 113, further comprising the act of [:]

[a communication link coupled to the subpixel vector change circuit and communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit] making a product in response to process set forth in claim 113.

115. (Amended) A [system] process comprising the acts of:

[a first memory] storing prior pixel image information in a first memory , the prior pixel image information representing a prior image;

[a second memory] storing next pixel image information in a second memory, the next pixel image information representing a next image; and

[a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit] generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory.

116. (Amended) A [system] process as set forth in claim 115, further comprising the act of [:]

[a communication link coupled to the spatial interpolation circuit, the communication link communicating output image information] making a product in response to the 64-pixel blocks of spatial interpolation information [generated by the spatial interpolation circuit].

117. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ;

a scale factor input circuit generating scale factor input information;

a scale factor memory;

a writing circuit coupled to the scale factor memory and coupled to the scale factor input circuit, the writing circuit writing scale factor information into the scale factor memory in response to the scale factor input information; and

a scaling processor coupled to the spatial interpolation circuit and coupled to the scale factor memory, the scaling processor generating the scaled image information in response to the scale factor information stored in the scaled memory and in response to the spatial interpolation information generated by the spatial interpolation circuit.

118. (Amended) A system as set forth in claim 117, further comprising:

a communication link coupled to the [spatial interpolation circuit] scaling processor, the communication link communicating output image information in response to the [spatial interpolation] scaled image information generated by the [spatial interpolation circuit] scaling processor.

119. (Amended) A system as set forth in claim 117, further comprising:

[a communication link communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information]

an integrated circuit multilevel memory having a plurality of multilevel memory cells, each of the plurality of multilevel memory cells storing at least two digital bits of information in a plurality of levels;

an integrated circuit multilevel memory accessing circuit generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

the scaling processor generating the scaled image information in response to the accessed digital information generated by the integrated circuit multilevel memory accessing circuit.

120. (Amended) A system as set forth in claim [117] 115, further comprising the acts of:

[a display circuit coupled to the spatial interpolation circuit and generating display image information in response to the spatial interpolation information generated by the spatial interpolation circuit; and

a display device coupled to the display circuit and displaying an image in response to the display image information generated by the display circuit]

storing at least two digital bits of information in a plurality of levels in each of a plurality of multilevel memory cells;

generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

generating the 64-pixel blocks of spatial interpolation information in response to the accessed digital information.

121. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a [spatial] temporal interpolation [circuit] processor generating [spatial interpolation] temporally interpolated image information by temporally interpolating in [response to] between the prior pixel image information [, the prior pixel image information representing a prior image,] and [in response to] the next pixel image information [, the next pixel image information representing a next image]; and

a subpixel vector change circuit generating subpixel vector change information [generated by the subpixel vector change circuit] having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information.

122. (Amended) A system as set forth in claim 121, further comprising:

a communication link [coupled to the spatial interpolation circuit, the communication link] communicating output image information in response to the [spatial interpolation] temporally interpolated image information [generated by the spatial interpolation circuit].

123. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit [coupled to the first memory and coupled to the second memory, the subpixel vector change circuit] generating subpixel vector change information [generated by the subpixel vector change circuit] having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory; [and]

a transform processor [coupled to the first memory and coupled to the second memory, the transform processor] generating 64-sample blocks of transformed image information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a weight input circuit generating weight input information;

a weight memory;

a writing circuit writing weight information into the weight memory in response to the weight input information; and

a weighting processor generating 64-sample blocks of weighted image information in response to the 64-sample blocks of transformed image information and in response to the weight information stored in the weight memory .

124. (Amended) A system as set forth in claim 123, further comprising:

a communication link [coupled to the transform processor, the communication link] communicating output image information in response to the [transformed] 64-sample blocks of weighted image information [generated by the transform processor].

125. (Amended) A [system] process comprising the acts of:

[a first memory] storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

[a second memory] storing next pixel image information in a second memory, the next pixel image information representing a next image; [and]

generating temporally interpolated image information in response to the to the prior pixel image information stored in the first memory and in response to the next pixel image information stored in the second memory; and

[a transform processor coupled to the first memory and coupled to the second memory, the transform processor] generating transformed image information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory.

126. (Amended) A [system] process as set forth in claim 125, further comprising the act of:

[a communication link coupled to the transform processor, the communication link] communicating output image information in response to the transformed image information [generated by the transform processor].

127. A [system] process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image; and

[a transform processor] generating 64-sample blocks of transformed image information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] .

128. A [system] process as set forth in claim 127, further comprising the act of:

[a communication link coupled to the transform processor, the communication link] communicating output image information in response to the 64-sample blocks of transformed image information [generated by the transform processor].

129. A [system] process as set forth in claim 127, further comprising the act of [:]

[a communication link communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information] making a product in response to the [next pixel] 64-sample blocks of transformed image information.

130. (Amended) A [system] process as set forth in claim [127] 125, further comprising the act of [:]

[a display circuit coupled to the transform processor and generating display image information in response to the transformed image information generated by the transform processor; and

a display device coupled to the display circuit and displaying an image in response to the display image information generated by the display circuit] making a product.

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131. (Amended) A system comprising:

a memory storing pixel image information;

a subpixel [vector] change circuit generating subpixel [vector] change information having subpixel resolution by subtracting in response to [prior] the pixel image information [, the prior pixel image information representing a prior image,] and in response to [next pixel image information, the next pixel image] feedback information [representing a next image]; [and]

a transform processor generating transformed image information in response to the [prior] pixel image information [and in response to the next pixel image information];

a scale factor input circuit generating scale factor input information;

a scale factor memory;

a writing circuit writing scale factor information into the scale factor memory, the scale factor memory storing the scale factor information;

a scaling processor generating scaled image information in response to the transformed image information and in response to the scale factor information; and

a feedback processor generating the feedback information in response to the scaled image information.

132. (Amended) A system as set forth in claim 131, further comprising:

a communication link [coupled to the transform processor, the communication link] communicating output image information in response to the transformed image information [generated by the transform processor].

133. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a [spatial] temporal interpolation [circuit] processor coupled to the first memory and coupled to the second memory, the [spatial] temporal interpolation [circuit] processor generating [spatial interpolation] 64-pixel blocks of temporally interpolated image information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory; and

a transform processor coupled to the [spatial] temporal interpolation [circuit] processor, the transform processor generating 64-sample blocks of transformed image information in response to the 64-pixel blocks of temporally interpolated image [spatial interpolation] information generated by the [spatial] temporal interpolation [circuit] processor.

134. (Amended) A system as set forth in claim 133, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the 64-sample blocks of transformed image information generated by the transform processor.

135. (Amended) A system comprising:

a first frame memory storing prior frame of image information;

a second frame memory storing next frame of image information;

a [spatial] temporal interpolation [circuit] processor generating a temporally interpolated frame of image [spatial interpolation] information in response to the prior [pixel] frame of image information [, the prior pixel image information representing a prior image,] and in response to the next [pixel] frame of image information [, the next pixel image information representing a next image]; and

a transform processor coupled to the [spatial] temporal interpolation [circuit] processor, the transform processor generating a frame of transformed image information in response to [spatial interpolation] the frame of temporally interpolated image information generated by the [spatial] temporal interpolation [circuit] processor.

136. (Amended) A system as set forth in claim 135, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the frame of transformed image information generated by the transform processor.

137. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit generating 64-pixel block of spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,]and in response to the next pixel image information [, the next pixel image information representing a next image];

a subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information; [and]

a transform processor [coupled to the spatial interpolation circuit, the transform processor] generating transformed image information in response to the spatial interpolation information [generated by the spatial interpolation circuit];

a weight input circuit generating weight input information;

a weight memory;

a writing circuit writing weight information into the weight memory in response to the weight input information, the weight memory storing the weight information; and

a weighting processor generating weighted image information in response to the transformed image information and in response to the weight information stored in the weight memory.

138. (Amended) A system as set forth in claim 137, further comprising:

a communication link [coupled to the transform processor, the communication link] communicating output image information in response to the [transformed] weighted image information [generated by the transform processor].

139. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit [coupled to the first memory and coupled to the second memory, the spatial interpolation circuit] generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a subpixel vector change circuit [coupled to the first memory and coupled to the second memory, the subpixel vector change circuit] generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit [coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit] generating scaled weighted image information in response to the spatial interpolation information [generated by the spatial interpolation circuit], in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit]; and

a resolution reduction circuit [coupled to the weighting and scaling circuit, the resolution reduction circuit] generating reduced resolution image information in response to the scaled weighted image information [generated by the weighting and scaling circuit].

140. (Amended) A system as set forth in claim 139, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the reduced resolution image information [generated by the resolution reduction circuit].

141. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit [coupled to the first memory and coupled to the second memory, the subpixel vector change circuit] generating subpixel vector change information [generated by the subpixel vector change circuit] having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information; and

a weighting and scaling circuit [coupled to the scale factor circuit, coupled to the weight circuit, coupled to the first memory and coupled to the second memory, the weighting and scaling circuit] generating scaled weighted image information in response to the prior pixel image information stored [by] in the first memory, in response to the next pixel image information stored [by] in the second memory, in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit] [; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

142. (Amended) A system as set forth in claim 141, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] weighted scaled image information [generated by the resolution reduction circuit].

143. (Amended) A [system] process comprising the acts of:

[a first memory] storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

[a second memory] storing next pixel image information in a second memory, the next pixel image information representing a next image;

[a weight circuit] generating weight information;

[a scale factor circuit] generating scale factor information; and

[a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, coupled to the first memory and coupled to the second memory, the weighting and scaling circuit] generating 64-sample blocks of scaled weighted image information in response to the prior pixel image information stored [by] in the first memory, in response to the next pixel image information stored [by] in the second memory, in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit ; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

144. (Amended) A [system] process as set forth in claim 143, further comprising the act of:

[a communication link coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] 64-sample blocks of weighted scaled image information [generated by the resolution reduction circuit].

145. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a weight circuit generating weight information;

a scale factor input circuit generating scale factor input information;

a scale factor memory;

a writing circuit writing scale factor information into the scale memory in response to the scale factor input information; and

a [weighting and] scaling [circuit coupled to the scale factor circuit and coupled to the weight circuit, the weighting and scaling circuit] processor generating scaled [weighted] image information in response to the prior pixel image information, in response to the next pixel image information, and in response to the scale factor information [generated by the] stored in the scale factor [circuit] memory [, and in response to the weight information generated by the weight circuit, the prior pixel image information representing a prior image and the next pixel image information representing a next image; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

146. (Amended) A system as set forth in claim 145, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled image information [generated by the resolution reduction circuit].

147. (Amended) A [system] process as set forth in claim [145] 143, further comprising the act of [:]

[a communication link communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information] making a product in response to the process set forth in claim 143.

148. (Amended) A system as set forth in claim 145, further comprising:

[a display circuit coupled to the resolution reduction circuit, the display circuit generating display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

a display device coupled to the display circuit, the display device displaying an image in response to the display image information generated by the display circuit]

an integrated circuit multilevel memory having a plurality of multilevel memory cells, each of the plurality of multilevel memory cells storing at least two digital bits of information in a plurality of levels;

an integrated circuit multilevel memory accessing circuit generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

the scaling processor generating the scaled image information in response to the accessed digital information generated by the integrated circuit multilevel memory accessing circuit.

149. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image];

a weight circuit generating weight information;

a scale factor circuit generating scale factor information; and

a weighting and scaling circuit coupled to the scale factor circuit and coupled to the weight circuit, the weighting and scaling circuit generating scaled weighted image information in response to the prior pixel image information, in response to the next pixel image information, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit[; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

150. (Amended) A system as set forth in claim 149, further comprising:

a communication link coupled to the [resolution reduction] weighting and scaling circuit, the communication link communicating output image information in response to the [reduced resolution] scaled weighted image information generated by the [resolution reduction] weighting and scaling circuit.

151. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit [coupled to the first memory and coupled to the second memory, the spatial interpolation circuit] generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

[a weight circuit generating weight information;]

a scale factor input circuit generating scale factor information;

a scale factor memory; and

a [weighting and] scaling [circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit] processor generating scaled [weighted] image information in response to the spatial interpolation information [generated by the spatial interpolation circuit,] and in response to the scale factor information [generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

152. (Amended) A system as set forth in claim 151, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled image information [generated by the resolution reduction circuit].

153. (Amended) A [system] process comprising the acts of:

storing pixel image information in a memory;

[a spatial interpolation circuit] generating spatial interpolation information in response to [prior ] the pixel image information [, the prior pixel image information representing a prior image,] and in response to [next pixel image] feedback information [, the next pixel image information representing a next image];

[a weight circuit] generating weight information;

[a scale factor circuit] generating scale factor information;

[a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit]

generating scaled weighted image information in response to the spatial interpolation information [generated by the spatial interpolation circuit], in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit]; and

generating the feedback information in response to the scaled weighted image information

[a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

154. (Amended) A [system] process as set forth in claim 153, further comprising the act of:

[a communication link coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled weighted image information [generated by the resolution reduction circuit].

155. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image];

a subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

a weight circuit generating weight information; and

[a scale factor circuit generating scale factor information;]

a weighting [and scaling] circuit [coupled to the scale factor circuit,] coupled to the weight circuit [,] and coupled to the spatial interpolation circuit, the weighting [and scaling] circuit generating [scaled] weighted image information in response to the spatial interpolation information generated by the spatial interpolation circuit [, in response to the scale factor information generated by the scale factor circuit,] and in response to the weight information generated by the weight circuit [; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

156. (Amended) A system as set forth in claim 155, further comprising:

a communication link coupled to the [resolution reduction] weighting circuit, the communication link communicating output image information in response to the [reduced resolution] weighted image information generated by the [resolution reduction] weighting circuit.

157. (Amended) A [system] process comprising the acts of:

[a first memory] storing [prior] pixel image information [, the prior pixel image information representing a prior image] in a memory;

[a second memory storing next pixel image information, the next pixel image information representing a next image;]

[a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit] generating subpixel delta [vector change] information [generated by the subpixel vector change circuit] having subpixel resolution by subtracting in response to the [prior] pixel image information [stored by the first memory] and in response to [the next pixel image] feedback information [stored by the second memory];

[a transform processor coupled to the first memory and coupled to the second memory, the transform processor] generating transformed image information in response to the [prior] pixel image information [stored by the first memory and in response to the next pixel image information stored by the second memory];

[a weight circuit] generating weight information;

[a scale factor circuit] generating scale factor information;

[a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit] generating scaled weighted image information in response to the transformed image information [generated by the transform processor], in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit]; and

[a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information] generating the feedback information in response to the scaled weighted image information [generated by the weighting and scaling circuit].

158. (Amended) A [system] process as set forth in claim 157, further comprising the act of:

[a communication link coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled weighted image information [generated by the resolution reduction circuit].

159. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a transform processor [coupled to the first memory and coupled to the second memory, the transform processor] generating transformed image information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information; and

a weighting and scaling circuit [coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit] generating scaled weighted image information in response to the transformed image information [generated by the transform processor], in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

160. (Amended) A system as set forth in claim 159, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled weighted image information [generated by the resolution reduction circuit].

161. (Amended) A [system] process comprising the acts of:

[a first memory] storing pixel image information in a memory;

[a transform] generating transformed image information in response to [prior] the pixel image information [, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image]and in response to feedback information;

[a weight circuit] generating weight information;

[a scale factor circuit] generating scale factor information;

[a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit] generating scaled weighted image information in response to the transformed image information [generated by the transform processor], in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit]; and

[a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image] generating the feedback information in response to the scaled weighted image information [generated by the weighting and scaling circuit].

162. (Amended) A [system] process as set forth in claim 161, further comprising the act of:

[a communication link coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled weighted image information [generated by the resolution reduction circuit].

163. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image];

a transform processor generating 64-sample blocks of transformed image information in response to the prior pixel image information and in response to the next pixel image information;

a weight circuit generating weight information;

a scale factor input circuit generating scale factor input information;

a scale factor memory;

a writing circuit writing scale factor information into the scale factor memory in response to the scale factor input information, the scale factor memory storing the scale factor information; and

a weighting and scaling circuit [coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit] generating 64-sample blocks of scaled weighted image information in response to the 64-sample blocks of transformed image information [generated by the transform processor], in response to the scale factor information [generated by] stored in the scale factor [circuit] memory, and in response to the weight information [generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

164. (Amended) A system as set forth in claim 163, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] 64-sample blocks of scaled weighted image information [generated by the resolution reduction circuit].

165. (Amended) A [system] process comprising the acts of:

[a first memory] storing [prior] pixel image information [, the prior pixel image information representing a prior image] in a memory;

[a second memory storing next pixel image information, the next pixel image information representing a next image;]

[a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit] generating spatial interpolation information in response to the [prior] pixel image information stored [by] in the [first] memory and in response to [the next pixel image] feedback information [stored by the second memory];

[a transform processor coupled to the spatial interpolation circuit, the transform processor] generating transformed image information in response to the spatial interpolation information [generated by the spatial interpolation circuit];

[a weight circuit] generating weight information;

[a scale factor circuit] generating scale factor information;

[a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit] generating scaled weighted image information in response to the transformed image information [generated by the transform processor], in response to the scale factor information [generated by the scale factor circuit], and in response to the weight information [generated by the weight circuit]; and

generating the feedback information in response to the scaled weighted image information

[a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

166. (Amended) A [system] process as set forth in claim 165, further comprising the act of [:]

[a communication link coupled to the resolution reduction circuit, the communication link communicating output image information] making a product in response to the [reduced resolution] scaled weighted image information [generated by the resolution reduction circuit].

167. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information [, the prior pixel image information representing a prior image,] and in response to next pixel image information [, the next pixel image information representing a next image] ;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information; and

[a scale factor circuit generating scale factor information;]

a weighting [and scaling] circuit [coupled to the scale factor circuit,] coupled to the weight circuit [,] and coupled to the transform processor, the weighting [and scaling] circuit generating [scaled] weighted image information in response to the transformed image

information generated by the transform processor [, in response to the scale factor information generated by the scale factor circuit,] and in response to the weight information generated by the weight circuit [; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

168. (Amended) A system as set forth in claim 167, further comprising:

a communication link coupled to the [resolution reduction] weighting circuit, the communication link communicating output image information in response to the [reduced resolution] weighted image information generated by the [resolution reduction] weighting circuit.

169. (Amended) A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image];

a subpixel vector change generating subpixel vector change information [generated by the subpixel vector change circuit] having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

a transform processor [coupled to the spatial interpolation circuit, the transform processor] generating transformed image information in response to the spatial interpolation information [generated by the spatial interpolation circuit];

a weight circuit generating weight information;

a scale factor input circuit generating scale factor input information;

a scale factor memory;

a writing circuit writing scale factor information into the scale factor memory in response to the scale factor input information; and

a weighting and scaling circuit [coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit] generating scaled weighted image information in response to the transformed image information [generated by the transform processor], in response to the scale factor information [generated by] stored in the scale factor [circuit] memory, and in response to the weight information [generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit].

170. (Amended) A system as set forth in claim 169, further comprising:

a communication link [coupled to the resolution reduction circuit, the communication link] communicating output image information in response to the [reduced resolution] scaled weighted image information [generated by the resolution reduction circuit].

171. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating subpixel vector change information [generated by the subpixel vector change circuit] having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating 64-sample blocks of transformed image information in response to the 64-pixel blocks of spatial interpolation information;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory;

generating 64-sample blocks of scaled weighted image information in response to the 64-sample blocks of transformed image information, in response to the scale factor information, and in response to the weight information stored in the weight memory; and

generating 64-sample blocks of reduced resolution image information in response to the 64-sample blocks of scaled weighted image information.

172. (Amended) A process as set forth in claim 171, further comprising the act of:

communicating output image information in response to the 64-sample blocks of reduced resolution image information.

173. (Amended) A process as set forth in claim 171, further comprising the act of [:]

[communicating output subpixel vector information in response to the subpixel vector change information] making a product.

187. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating subpixel vector change information [generated by the subpixel vector change circuit] having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory; and

generating 64-sample blocks of transformed image information in response to the 64-pixel blocks of spatial interpolation information.

188. (Amended) A process as set forth in claim 187, further comprising the act of:

communicating output image information in response to the [spatial interpolation] 64-sample blocks of transformed image information.

189. (Amended) A process as set forth in claim 187, further comprising the act of:

making a product in response to the [spatial interpolation information] process set forth in claim 187.

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190. (Amended) A process comprising the acts of:

storing [prior] pixel image information in a [first] memory [, the prior pixel image information representing a prior image];

[storing next pixel image information in a second memory, the next pixel image information representing a next image];

generating spatial interpolation information in response to the [prior] pixel image information [stored by the first memory and in response to the next pixel image information] stored [by] in the [second] memory; [and]

generating subpixel [vector] change image information [generated by the subpixel vector change circuit] having subpixel resolution by subtracting in response to the [prior] pixel image information stored [by] in the [first] memory and in response to [the next pixel image] feedback information [stored by the second memory]; and

generating the feedback information in response to the subpixel change image information.

191. (Amended) A process as set forth in claim 190, further comprising the act of:

communicating output image information [in response to the spatial interpolation information].

192. (Amended) A process as set forth in claim 190, further comprising the act of:

making a product in response to the [spatial interpolation information] process set forth in claim 190.

193. (Amended) A process comprising the acts of:

storing [prior] pixel image information in a [first] memory [, the prior pixel image information representing a prior image];

[storing next pixel image information in a second memory, the next pixel image information representing a next image; and]

generating delta subpixel [vector change] image information [generated by the subpixel vector change circuit] having subpixel resolution by subtracting in response to the [prior] pixel image information stored [by] in the [first] memory and in response to [the next pixel image] feedback information [stored by the second memory]; and

generating the feedback information in response to the delta subpixel image information.

194. (Amended) A process as set forth in claim 193, further comprising the act of:

communicating output image information in response to the [prior] pixel image information stored [by] in the [first] memory [and in response to the next pixel image information stored by the second memory].

195. (Amended) A process as set forth in claim 193, further comprising the act of [:]

[communicating output subpixel vector information] making a product in response to the delta subpixel [vector change] image information.

196. (Amended) A process as set forth in claim 193, further comprising the acts of:

[generating display image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

displaying an image in response to the display image information]

storing at least two digital bits of information in a plurality of levels in each of a plurality of multilevel memory cells;

generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

generating the delta subpixel image information in response to the accessed digital information.

197. (Amended) A process as set forth in claim [193] 187, further comprising the acts of:

[making a product in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory]

storing at least two digital bits of information in a plurality of levels in each of a plurality of multilevel memory cells;

generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

generating the 64-sample blocks of transformed image information in response to the accessed digital information.

198. (Amended) A process comprising the acts of:

storing pixel image information in a memory;

generating subpixel [vector change] difference image information having subpixel resolution in response to [prior] the pixel image information [, the prior pixel image information representing a prior image,] and in response to [next pixel image] feedback information [, the next pixel image information representing a next image]; and

generating the feedback information in response to the subpixel difference image information.

199. (Amended) A process as set forth in claim 198, further comprising the act of:

communicating output [subpixel vector] image information in response to the subpixel [vector change] difference image information.

200. (Amended) A process as set forth in claim 198, further comprising the act of:

making a product in response to the [subpixel vector change information] process set forth in claim 198.

201. (Amended) A process comprising the acts of:

storing [prior] pixel image information in a [first] memory [, the prior pixel image information representing a prior image];

[storing next pixel image information in a second memory, the next pixel image information representing a next image; and]

generating 64-pixel blocks of spatial interpolation information in response to the [prior] pixel image information stored [by] in the [first] memory and in response to [the next pixel image] feedback information [stored by the second memory];

generating weight input information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory;

generating 64-sample blocks of weighted image information in response to the 64-pixel blocks of spatial interpolation information and in response to the weight information stored in the weight memory; and

generating the feedback information in response to the 64-sample blocks of weighted image information.

202. (Amended) A process as set forth in claim 201, further comprising the act of:

communicating output image information in response to the 64-pixel blocks of spatial interpolation information.

203. (Amended) A process as set forth in claim 201, further comprising the act of:

making a product [in response to the spatial interpolation information].

204. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ;

generating scale factor input information;

writing scale factor information into a scale memory in response to the scale factor input information;

storing the scale factor information in the scale memory; and

generating 64-sample blocks of scaled image information in response to the 64-pixel blocks of spatial interpolation information and in response to the scale factor information stored in the scale memory.

205. (Amended) A process as set forth in claim 204, further comprising the act of:

communicating output image information in response to the 64-pixel blocks of spatial interpolation information.

206. (Amended) A process as set forth in claim 204, further comprising the act of [:]

[communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information] making a product.

207. (Amended) A process as set forth in claim 204, further comprising the acts of:

[generating display image information in response to the spatial interpolation information; and

displaying an image in response to the display image information]

storing at least two digital bits of information in a plurality of levels in each of a plurality of multilevel memory cells;

generating accessed digital information in response to the at least two digital bits of information stored in each of the plurality of multilevel memory cells; and

generating the 64-pixel blocks of spatial interpolation information in response to the accessed digital information.

208. (Amended) A process as set forth in claim 204, further comprising the act of:

making a manufactured product in response to the 64-pixel blocks of spatial interpolation information.

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209. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ; and

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information.

210. (Amended) A process as set forth in claim 209, further comprising the act of:

communicating output image information in response to the 64-pixel blocks of spatial interpolation information.

211. (Amended) A process as set forth in claim 209, further comprising the act of:

making a product in response to the 64-pixel blocks of spatial interpolation information.

212. (Amended) A process comprising the acts of:

storing a prior 64-pixel block of image information in a first memory, the prior 64-pixel block of image information representing a prior image;

storing a next 64-pixel block of image information in a second memory, the next 64-pixel block of image information representing a next image;

H3 generating a temporally interpolated 64-pixel block of image information by temporally interpolating in response to the prior 64-pixel block of image information stored in the first memory and in response to the next 64-pixel block of image information stored in the second memory;

generating subpixel vector change information having subpixel resolution in response to the prior 64-pixel block of image information stored [by] in the first memory and in response to the next 64-pixel block of image information stored [by] in the second memory; and

generating 64-sample blocks of transformed image information in response to the prior 64-pixel block of image information stored [by] in the first memory and in response to the next 64-pixel block of image information stored [by] in the second memory.

213. (Amended) A process as set forth in claim 212, further comprising the act of:

communicating output image information in response to the 64-sample blocks of transformed image information.

214. (Amended) A process as set forth in claim 212, further comprising the act of:

making a product in response to the 64-sample blocks of transformed image information.

215. (Amended) A process comprising the acts of:

storing [prior] pixel image information in a [first] memory[, the prior pixel image information representing a prior image];

[storing next pixel image information in a second memory, the next pixel image information representing a next image; and]

generating transformed image information in response to the [prior] pixel image information stored [by] in the [first] memory and in response to [the next pixel image] feedback information [stored by the second memory] ; and

generating the feedback information in response to the transformed image information.

216. (Amended) A process as set forth in claim 215, further comprising the act of:

communicating output image information in response to the [transformed] pixel image information stored in the memory.

217. (Amended) A process as set forth in claim 215, further comprising the act of:

making a product [in response to the transformed image information].

218. (Amended) A process comprising the acts of:

storing pixel image information in a memory;

generating transformed image information in response to [prior] pixel image information [, the prior pixel image information representing a prior image,] and in response to [next pixel image] feedback information [, the next pixel image information representing a next image];

generating scale factor input information;

writing scale factor information into a scale memory in response to the scale factor input information;

storing the scale factor information in the scale memory;

generating scaled image information in response to the transformed image information and in response to the scale factor information stored in the scale memory; and

generating the feedback information in response to the scaled image information.

219. (Amended) A process as set forth in claim 218, further comprising the act of [:] [communicating output image information] making a product in response to the transformed image information.

220. (Amended) A process as set forth in claim 218, further comprising the act of:

communicating output [prior pixel] image information in response to the [prior pixel image information and communicating output next pixel image information in response to the next pixel] transformed image information.

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221. (Amended) A process as set forth in claim 218, further comprising the acts of:

[generating display image information] making a design product in response to the transformed image information; and

[displaying an image] making a second product in response to the [display image information] design product.

222. (Amended) A process as set forth in claim 218, further comprising the act of:

making a signal product in response to the transformed image information.

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223. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ; and

generating 64-sample blocks of transformed image information in response to the prior pixel image information and in response to the next pixel image information.

224. (Amended) A process as set forth in claim 223, further comprising the act of:

communicating output image information in response to the 64-sample blocks of transformed image information.

225. (Amended) A process as set forth in claim 223, further comprising the act of:

making a product in response to the 64-sample blocks of transformed image information.

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226. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory; and

generating transformed image information in response to the spatial interpolation information.

227. (Amended) A process as set forth in claim 226, further comprising the act of:

communicating output image information in response to the [transformed] spatial interpolation [image] information.

228. (Amended) A process as set forth in claim 226, further comprising the act of:

making a product [in response to the transformed image information].

229. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ; and

generating 64-sample blocks of transformed image information in response to the 64-pixel blocks of spatial interpolation information.

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230. (Amended) A process as set forth in claim 229, further comprising the act of:

communicating output image information in response to the 64-sample blocks of transformed image information.

231. (Amended) A process as set forth in claim 229, further comprising the act of:

making a product in response to the 64-sample blocks of transformed image information.

232. (Amended) A process comprising the acts of:

storing pixel image information in a memory;

generating 64-pixel blocks of spatial interpolation information in response to [prior] the pixel image information [, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image];

generating delta subpixel [vector change] information having subpixel resolution in response to the [prior] pixel image information and in response to [the next pixel image] feedback information; [and]

generating 64-sample blocks of transformed image information in response to 64-pixel blocks of spatial interpolation information; and

generating the feedback information in response to the 64-sample blocks of transformed image information.

233. (Amended) A process as set forth in claim 232, further comprising the act of:

communicating output image information in response to the 64-sample blocks of transformed image information.

234. (Amended) A process as set forth in claim 232, further comprising the act of:

making a product in response to the 64-sample blocks of transformed image information.

235. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information stored in the weight memory[; and

generating reduced resolution image information in response to the scaled weighted image information].

236. (Amended) A process as set forth in claim 235, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

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237. (Amended) A process as set forth in claim 235, further comprising the act of:

making a product in response to the [reduced resolution] scaled weighted image information.

238. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating weight information; and

[generating scale factor information;]

generating [scaled] weighted image information in response to the prior pixel image information stored [by] in the first memory, in response to the next pixel image information stored [by] in the second memory [, in response to the scale factor information], and in response to the weight information[; and]

[generating reduced resolution image information in response to the scaled weighted image information].

239. (Amended) A process as set forth in claim 238, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled image information.

240. (Amended) A process as set forth in claim 238, further comprising the act of:

making a product in response to the [reduced resolution] scaled image information.

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241. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating scaled weighted image information in response to the prior pixel image information stored [by] in the first memory, in response to the next pixel image information stored [by] in the second memory, in response to the scale factor information, and in response to the weight information stored in the weight memory[; and

generating reduced resolution image information in response to the scaled weighted image information].

242. (Amended) A process as set forth in claim 241, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

243. (Amended) A process as set forth in claim 241, further comprising the act of:

making a product in response to the [reduced resolution] scaled weighted image information.

244. (Amended) A process comprising the acts of:

storing a prior 64-pixel block of pixel image information in a first memory;

storing a next 64-pixel block of pixel image information in a second memory;

generating temporally interpolated 64-pixel block of image information by temporally interpolating in between the prior 64-pixel block of pixel image information and the next 64-pixel block of pixel image information; [, the prior pixel image information representing a prior image and the next pixel image information representing a next image];

generating weight information;

generating scale factor information; and

generating 64-sample blocks of scaled weighted image information in response to the prior 64-pixel block of pixel image information, in response to the next 64-pixel block of pixel image information, in response to the scale factor information, and in response to the weight information [, the prior pixel image information representing a prior image and the next pixel image information representing a next image ; and

generating reduced resolution image information in response to the scaled weighted image information].

245. (Amended) A process as set forth in claim 244, further comprising the act of:

communicating output image information in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

246. (Amended) A process as set forth in claim 244, further comprising the act of [:]

[communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information] making a disk product in response to the [next pixel] 64 sample blocks of scaled weighted image information.

247. (Amended) A process as set forth in claim 244, further comprising the acts of:

[generating display image information in response to the reduced resolution image information] making a computer aided design product; and

[displaying an image] making a second product in response to the [display image information] computer aided design product.

248. (Amended) A process as set forth in claim 244, further comprising the act of:

making a product [in response to the reduced resolution image information].

249. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory;

generating scaled weighted image information in response to the prior pixel image information, in response to the next pixel image information, in response to the scale factor information, and in response to the weight information stored in the weight memory; and

generating reduced resolution image information in response to the scaled weighted image information.

250. (Amended) A process as set forth in claim 249, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

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251. (Amended) A process as set forth in claim 249, further comprising the act of:

making a product in response to the [reduced resolution image information] process set forth in claim 249.

252. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information stored in the weight memory [; and

generating reduced resolution image information in response to the scaled weighted image information].

253. (Amended) A process as set forth in claim 252, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

254. (Amended) A process as set forth in claim 252, further comprising the act of:

making a product in response to the [reduced resolution] scaled weighted image information.

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255. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image] ;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating 64-sample blocks of scaled weighted image information in response to the 64-pixel blocks of spatial interpolation information, in response to the scale factor information, and in response to the weight information stored in the weight memory [; and

generating reduced resolution image information in response to the scaled weighted image information].

256. (Amended) A process as set forth in claim 255, further comprising the act of:

communicating output image information in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

257. (Amended) A process as set forth in claim 255, further comprising the act of:

making a product in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

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258. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image, ]and in response to the next pixel image information [, the next pixel image information representing a next image];

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

generating weight information;

generating scale factor information; and

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information [; and

generating reduced resolution image information in response to the scaled weighted image information].

259. (Amended) A process as set forth in claim 258, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

260. (Amended) A process as set forth in claim 258, further comprising the act of:

making a product in response to the [reduced resolution] scaled weighted image information.

261. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating transformed image information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information stored in the weight memory[; and

generating reduced resolution image information in response to the scaled weighted image information].

262. (Amended) A process as set forth in claim 261, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

263. (Amended) A process as set forth in claim 261, further comprising the act of:

making a product in response to the [reduced resolution] scaled weighted image information.

264. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating transformed image information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating weight information; and

[generating scale factor information;]

generating [scaled] weighted image information in response to the transformed image information[, in response to the scale factor information,] and in response to the weight information; [and

generating reduced resolution image information in response to the scaled weighted image information].

265. (Amended) A process as set forth in claim 264, further comprising the act of:

communicating output image information in response to the [reduced resolution] weighted image information.

266. (Amended) A process as set forth in claim 264, further comprising the act of:

making a product in response to the [reduced resolution] weighted image information.

267. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

[a transform] generating 64-sample blocks of transformed image information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image];

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating 64-sample blocks of scaled weighted image information in response to the 64-sample blocks of transformed image information, in response to the scale factor information, and in response to the weight information stored in the weight memory [; and

generating reduced resolution image information in response to the scaled weighted image information].

268. (Amended) A process as set forth in claim 267, further comprising the act of:

communicating output image information in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

269. (Amended) A process as set forth in claim 267, further comprising the act of:

making a product in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

270. (Amended) A process comprising the acts of:

storing pixel image information in a memory;

generating subpixel [vector change] difference information having subpixel resolution by subtracting in response to [prior] the pixel image information [, the prior pixel image information representing a prior image,] and in response to [next pixel image] feedback information [, the next pixel image information representing a next image];

generating transformed image information in response to the [prior] pixel image information [and in response to the next pixel image information];

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating the feedback information in response to the scaled weighted image information [; and

generating reduced resolution image information in response to the scaled weighted image information].

271. (Amended) A process as set forth in claim 270, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

272. (Amended) A process as set forth in claim 270, further comprising the act of:

making a product in response to the [reduced resolution] scaled weighted image information.

273. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

generating 64-sample blocks of transformed image information in response to 64-pixel blocks of spatial interpolation information;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating 64-sample blocks of scaled weighted image information in response to the 64-sample blocks of transformed image information, in response to the scale factor information, and in response to the weight information stored in the weight memory[; and

generating reduced resolution image information in response to the scaled weighted image information].

274. (Amended) A process as set forth in claim 273, further comprising the act of:

communicating output image information in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

275. (Amended) A process as set forth in claim 273, further comprising the act of:

making a product in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

276. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory;

storing next pixel image information in a second memory;

generating [spatial] temporally interpolated image [interpolation] information in [response to] between the prior pixel image information [, the prior pixel image information representing a prior image,] and [in response to] the next pixel image information [, the next pixel image information representing a next image];

generating transformed image information in response to [spatial] the temporally interpolated image [interpolation] information;

generating weight information;

generating scale factor information; and

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information [; and

generating reduced resolution image information in response to the scaled weighted image information].

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277. (Amended) A process as set forth in claim 276, further comprising the act of:

communicating output image information in response to the [reduced resolution] scaled weighted image information.

278. (Amended) A process as set forth in claim 276, further comprising the act of:

making a product in response to the [reduced resolution image information] process set forth in claim 276.

279. (Amended) A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating 64-pixel blocks of spatial interpolation information in response to the prior pixel image information [, the prior pixel image information representing a prior image,] and in response to the next pixel image information [, the next pixel image information representing a next image];

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

generating 64-sample blocks of transformed image information in response to the 64-pixel blocks of spatial interpolation information;

generating weight input information;

generating scale factor information;

writing weight information into a weight memory in response to the weight input information;

storing the weight information in the weight memory; and

generating 64-sample blocks of scaled weighted image information in response to the 64-sample blocks of transformed image information, in response to the scale factor information, and in response to the weight information stored in the weight memory[; and

generating reduced resolution image information in response to the scaled weighted image information].

280. (Amended) A process as set forth in claim 279, further comprising the act of:

communicating output image information in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

281. (Amended) A process as set forth in claim 279, further comprising the act of:

making a product in response to the [reduced resolution] 64-sample blocks of scaled weighted image information.

284. (Amended) A system as set forth in claim 98,

wherein the spatial interpolation circuit includes a spatial interpolation processor circuit for generating the spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the subpixel vector change circuit includes a subpixel vector change processor circuit generating the subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the weight circuit includes a weight processor circuit for generating the weight information;

wherein the scale factor circuit includes a scale factor processor circuit for generating the scale factor information;

wherein the weighting and scaling circuit includes a weighting and scaling processor circuit for generating the scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit includes a resolution reduction processor circuit for generating the reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit; and

wherein the display circuit includes a display processor circuit for generating the display image information in response to the reduced resolution image information generated by the resolution reduction circuit.

285. (Amended) A system as set forth in claim 98,

wherein the first memory includes a plurality of first memories for storing the prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory includes a plurality of second memories for storing the next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit includes a plurality of spatial interpolation circuits for generating the spatial interpolation information in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the subpixel vector change circuit includes a plurality of subpixel vector change circuits for generating the subpixel vector change information having subpixel resolution in response to the prior pixel image information stored [by] in the first memory and in response to the next pixel image information stored [by] in the second memory;

wherein the transform processor includes a plurality of transform processors for generating the transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit includes a plurality of weight circuits for generating the weight information;

wherein the scale factor circuit includes a plurality of scale factor circuits for generating the scale factor information;

wherein the weighting and scaling circuit includes a plurality of weighting and scaling circuits for generating the scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit includes a plurality of resolution reduction circuits for generating the reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link includes a plurality of image communication links for communicating the output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link includes a plurality of vector communication links for communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit;

wherein the display circuit includes a plurality of display circuits for generating the display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device includes a plurality of display devices for displaying the image in response to the display image information generated by the display circuit.

Please add new claims 380 - 510, as follows:

--380. A system comprising:

memory means for storing pixel image information;

means for generating weight information;

means for generating scale factor information; and

means for generating scaled weighted image information in response to the pixel image information stored in the memory means, in response to the scale factor information, and in response to the weight information.

--381. A system comprising:

memory means for storing a prior 64-pixel block of image information;

memory means for storing a next 64-pixel block of image information;

means for generating a plurality of temporally interpolated 64-pixel blocks of image information in between the prior 64-pixel block of image information and the next 64-pixel block of image information; and

means for generating transformed image information in response to the plurality of temporally interpolated 64-pixel blocks of image information.

--382. A system comprising:

memory means for storing pixel image information;

means for generating spatial interpolation information in response to the pixel image information stored in the memory means;

means for generating subpixel difference image information having subpixel resolution by subtracting in response to the pixel image information stored in the memory means and in response to feedback information;

means for generating weight input information;

weight memory means;

means for writing weight information into the weight memory in response to the weight input information, the weight memory means storing the weight information;

means for generating weighted image information in response to the weight information stored in the weight memory means and in response to the spatial interpolation information; and

means for generating the feedback information in response to the weighted image information.

--383. A system comprising:

memory means for storing a prior 64-pixel block of image information;

memory means for storing a next 64-pixel block of image information;

means for generating a first temporally interpolated 64-pixel block of image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

means for generating a second temporally interpolated 64-pixel block of image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

means for generating a third temporally interpolated 64-pixel block of image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

means for generating first transformed image information in response to the first temporally interpolated 64-pixel block of image information;

means for generating second transformed image information in response to the second temporally interpolated 64-pixel block of image information; and

means for generating third transformed image information in response to the third temporally interpolated 64-pixel block of image information.

--384. A system comprising:

memory means for storing a prior 64-pixel block of image information;

memory means for storing a next 64-pixel block of image information;

means for generating first temporally interpolated image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

means for generating second temporally interpolated image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

means for generating third temporally interpolated image information by temporally interpolating in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

means for generating first transformed image information in response to the first temporally interpolated image information;

means for generating second transformed image information in response to the second temporally interpolated image information;

means for generating third transformed image information in response to the third temporally interpolated image information;

means for generating weight input information;

weight memory means;

means for writing weight information into the weight memory in response to the weight input information, the weight memory means storing the weight information;

means for generating first weighted image information in response to the weight information stored in the weight memory means and in response to the first transformed image information;

means for generating second weighted image information in response to the weight information stored in the weight memory means and in response to the second transformed image information; and

means for generating third weighted image information in response to the weight information stored in the weight memory means and in response to the third transformed image information.

--385. A process comprising the acts of:

storing a prior 64-pixel block of image information in a first memory, the prior 64-pixel block of image information representing a prior image;

storing a next 64-pixel block of image information in a second memory, the next 64-pixel block of image information representing a next image;

generating a temporally interpolated 64-pixel block of image information by temporally interpolating in between the in response to the prior 64-pixel block of image information stored in the first memory and in response to the next 64-pixel block of image information stored in the second memory;

generating subpixel vector change information having subpixel resolution in response to the prior 64-pixel block of image information stored in the first memory and in response to the next 64-pixel block of image information stored in the second memory;

generating 64-sample blocks of transformed image information in response to the prior 64-pixel block of image information stored in the first memory and in response to the next 64-pixel block of image information stored in the second memory; and

generating 64-sample blocks of reduced resolution image information in response to the 64-sample blocks of transformed image information.

--386. A process as set forth in claim 385, further comprising the act of making a product.

--387. A process as set forth in claim 385, further comprising the act of making a data compressed product in response to the 64-sample blocks of reduced resolution image information.

--388. A process as set forth in claim 385, further comprising the acts of:

making a display product in response to the process set forth in claim 385; and

making a second product in response to the display product.

--389. A process as set forth in claim 385, further comprising the acts of:

making a first product; and

making a second product in response to the first product.

--390. A process comprising the acts of:

storing pixel image information in a memory;

generating spatial interpolation information in response to the pixel image information and in response to feedback information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the spatial interpolation information, in response to the weight information, and in response to the scale factor information;

generating reduced resolution image information in response to the scaled weighted image information; and

generating the feedback information in response to the reduced resolution image information.

--391. A process as set forth in claim 390, further comprising the act of making a product in response to the spatial interpolation information.

--392. A process as set forth in claim 390, further comprising the act of making a building product in response to the process set forth in claim 390.

--393. A process as set forth in claim 390, further comprising the acts of:

making a display product; and

making a second product in response to the display product.

--394. A process as set forth in claim 390, further comprising the acts of:

making a first product in response to the spatial interpolation information;

making a second product in response to the first product; and

making a third product in response to the second product.

--395. A process comprising the acts of:

storing a prior 64-pixel block of image information in a first memory;

storing a next 64-pixel block of image information in a second memory;

generating a first temporally interpolated 64-pixel block of image information in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

generating a second temporally interpolated 64-pixel block of image information in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

generating a third temporally interpolated 64-pixel block of image information in between the prior 64-pixel block of image information and the next 64-pixel block of image information;

generating first reduced resolution image information in response to the first temporally interpolated 64-pixel block of image information;

generating second reduced resolution image information in response to the second temporally interpolated 64-pixel block of image information; and

generating third reduced resolution image information in response to the third temporally interpolated 64-pixel block of image information.

--396. A process as set forth in claim 395, further comprising the act of making a product in response to the process set forth in claim 395.

--397. A process as set forth in claim 395, further comprising the act of making a vehicle product.

--398. ~~A process as set forth in claim 395, further comprising the acts of:~~
making a design product; and
making a second product in response to the design product.

--399. A process as set forth in claim 395, further comprising the acts of:
making a first product in response to the process set forth in claim 395; and
making a second product in response to the first product.

--400. A process as set forth in claim 109, further comprising the act of making a communication product in response to the temporally interpolated image information.

--401. A process as set forth in claim 109, further comprising the acts of:
making a design product in response to the process set forth in claim 109; and
making a second product in response to the design product.

--402. A process as set forth in claim 109, further comprising the acts of:
making a first product; and
making a second product in response to the first product.

--403. A process as set forth in claim 113, further comprising the act of making a communicated product.

--404. A process as set forth in claim 113, further comprising the acts of:
making a display product; and
making a second product in response to the display product.

--405. A process as set forth in claim 113, further comprising the acts of:

making a first product;

making a second product in response to the first product; and

making a third product in response to the second product.

--406. A process as set forth in claim 115, further comprising the act of making a machined product in response to the process set forth in claim 115.

--407. A process as set forth in claim 115, further comprising the acts of:

making a computer aided design product; and

making a second product in response to the computer aided design product.

--408. A process as set forth in claim 115, further comprising the acts of:

making a first product in response to the 64-pixel blocks of spatial interpolation information; and

making a second product in response to the first product.

--409. A process as set forth in claim 125, further comprising the act of making a database product in response to the temporally interpolated image information.

--410. A process as set forth in claim 125, further comprising the acts of:

making a design product in response to the process set forth in claim 125; and

making a second product in response to the design product.

--411. A process as set forth in claim 125, further comprising the acts of:

making a first product in response to the temporally interpolated image information;

making a second product in response to the first product; and

making a third product in response to the second product.

--412. A process as set forth in claim 127, further comprising the act of making a filter product.

--413. A process as set forth in claim 127, further comprising the acts of:
making a display product in response to the 64-sample blocks of transformed image information; and
making a second product in response to the display product.

--414. A process as set forth in claim 127, further comprising the acts of:
making a first product in response to the process set forth in claim 127; and
making a second product in response to the first product.

--415. A process as set forth in claim 143, further comprising the act of making a graphic product in response to the process set forth in claim 143.

--416. A process as set forth in claim 143, further comprising the acts of:
making a computer aided design product; and
making a second product in response to the computer aided design product.

--417. A process as set forth in claim 143, further comprising the acts of:
making a first product in response to the process set forth in claim 143;
making a second product in response to the first product; and
making a third product in response to the second product.

--418. A process as set forth in claim 153, further comprising the act of making a data compressed database product in response to the scaled weighted image information.

--419. A process as set forth in claim 153, further comprising the acts of:
making a design product in response to the process set forth in claim 153; and
making a second product in response to the design product.

--420. A process as set forth in claim 153, further comprising the acts of:

making a first product; and

making a second product in response to the first product.

--421. A process as set forth in claim 157, further comprising the act of making a video product.

--422. A process as set forth in claim 157, further comprising the acts of:

making a display product in response to the scaled weighted image information; and

making a second product in response to the display product.

--423. A process as set forth in claim 157, further comprising the acts of:

making a first product;

making a second product in response to the first product; and

making a third product in response to the second product.

--424. A process as set forth in claim 161, further comprising the act of making a location product in response to the process set forth in claim 161.

--425. A process as set forth in claim 161, further comprising the acts of:

making a first product in response to the scaled weighted image information; and

making a second product in response to the first product.

--426. A process as set forth in claim 165, further comprising the act of making a designed product in response to the scaled weighted image information.

--427. A process as set forth in claim 165, further comprising the acts of:
making a design product in response to the process set forth in claim 165; and
making a second product in response to the design product.

--428. A process as set forth in claim 165, further comprising the acts of:
making a first product in response to the scaled weighted image information;
making a second product in response to the first product; and
making a third product in response to the second product.

--429. A process as set forth in claim 171, further comprising the act of making a telephone product.

--430. A process as set forth in claim 171, further comprising the acts of:
making a computer aided design product in response to the 64-sample blocks of reduced resolution image information; and
making a second product in response to the computer aided design product.

--431. A process as set forth in claim 171, further comprising the acts of:
making a first product in response to the process set forth in claim 171; and
making a second product in response to the first product.

--432. A process as set forth in claim 187, further comprising the act of making a machine product in response to the process set forth in claim 187.

--433. A process as set forth in claim 187, further comprising the acts of:
making a display product; and
making a second product in response to the display product.

--434. A process as set forth in claim 187, further comprising the acts of:
making a first product in response to the process set forth in claim 187;
making a second product in response to the first product; and
making a third product in response to the second product.

--435. A process as set forth in claim 190, further comprising the act of making an oil product.

506 I 30 --436. A process as set forth in claim 190, further comprising the acts of:
making a computer aided design product in response to the process set forth in claim 190; and
making a second product in response to the computer aided design product.

H5 --437. A process as set forth in claim 190, further comprising the acts of:
making a first product; and
making a second product in response to the first product.

--438. A process as set forth in claim 193, further comprising the act of making an animation product.

506 I 31 --439. A process as set forth in claim 193, further comprising the acts of:
making a design product in response to the pixel image information; and
making a second product in response to the design product.

--440. A process as set forth in claim 193, further comprising the acts of:
making a first product;
making a second product in response to the first product; and
making a third product in response to the second product.

--441. A process as set forth in claim 198, further comprising the act of making an architectural product in response to the process set forth in claim 198.

--442. A process as set forth in claim 198, further comprising the acts of:

making a display product; and

making a second product in response to the display product.

--443. A process as set forth in claim 198, further comprising the acts of:

making a first product in response to the subpixel difference image information; and

making a second product in response to the first product.

--444. A process as set forth in claim 201, further comprising the act of making an entertainment product in response to the 64-pixel blocks of spatial interpolation information.

--445. A process as set forth in claim 201, further comprising the acts of:

making a computer aided design product in response to the process set forth in claim 201; and

making a second product in response to the computer aided design product.

--446. A process as set forth in claim 201, further comprising the acts of:

making a first product in response to the 64-pixel blocks of spatial interpolation information;

making a second product in response to the first product; and

making a third product in response to the second product.

--447. A process as set forth in claim 204, further comprising the act of making an information product.

--448. A process as set forth in claim 204, further comprising the acts of:
making a first product in response to the process set forth in claim 204; and
making a second product in response to the first product.

--449. A process as set forth in claim 209, further comprising the act of making an electronic product in response to the process set forth in claim 209.

--450. A process as set forth in claim 209, further comprising the acts of:
making a first product in response to the process set forth in claim 209;
making a second product in response to the first product; and
making a third product in response to the second product.

--451. A process as set forth in claim 212, further comprising the act of making a television product in response to the 64-sample blocks of transformed image information.

--452. A process as set forth in claim 212, further comprising the acts of:
making a computer aided design product in response to the process set forth in claim 212; and
making a second product in response to the computer aided design product.

--453. A process as set forth in claim 212, further comprising the acts of:
making a first product; and
making a second product in response to the first product.

--454. A process as set forth in claim 215, further comprising the act of making a telephone product.

--455. A process as set forth in claim 215, further comprising the acts of:
making a design product in response to the transformed image information; and
making a second product in response to the design product.

--456. A process as set forth in claim 215, further comprising the acts of:

making a first product;

making a second product in response to the first product; and

making a third product in response to the second product.

--457. A process as set forth in claim 218, further comprising the act of making a data decompressed product in response to the process set forth in claim 218.

--458. A process as set forth in claim 218, further comprising the acts of:

making a first product in response to the scaled image information; and

making a second product in response to the first product.

--459. A process as set forth in claim 223, further comprising the act of making a geophysical product in response to the 64-sample blocks of transformed image information.

--460. A process as set forth in claim 223, further comprising the acts of:

making a computer aided design product in response to the process set forth in claim 223; and

making a second product in response to the computer aided design product.

--461. A process as set forth in claim 223, further comprising the acts of:

making a first product;

making a second product in response to the first product; and

making a third product in response to the second product.

--462. A process as set forth in claim 226, further comprising the act of making a natural resource product.

--463. A process as set forth in claim 226, further comprising the acts of:

making a design product in response to the transformed image information; and

making a second product in response to the design product.

--464. A process as set forth in claim 226, further comprising the acts of:

making a first product in response to the process set forth in claim 226; and

making a second product in response to the first product.

--465. A process as set forth in claim 229, further comprising the act of making a mineral product in response to the process set forth in claim 229.

--466. A process as set forth in claim 229, further comprising the acts of:

making a display product; and

making a second product in response to the display product.

--467. A process as set forth in claim 229, further comprising the acts of:

making a first product in response to the process set forth in claim 229;

making a second product in response to the first product; and

making a third product in response to the second product.

--468. A process as set forth in claim 232, further comprising the act of making a processed product in response to the 64-sample blocks of transformed image information.

--469. A process as set forth in claim 232, further comprising the acts of:

making a computer aided design product in response to the process set forth in claim 232; and

making a second product in response to the computer aided design product.

--470. A process as set forth in claim 232, further comprising the acts of:

making a first product; and

making a second product in response to the first product.

--471. A process as set forth in claim 235, further comprising the act of making a position product.

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--472. A process as set forth in claim 235, further comprising the acts of:

making a design product in response to the scaled weighted image information; and

making a second product in response to the design product.

--473. A process as set forth in claim 235, further comprising the acts of:

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making a first product;

making a second product in response to the first product; and

making a third product in response to the second product.

--474. A process as set forth in claim 238, further comprising the act of making a moving product in response to the process set forth in claim 238.

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--475. A process as set forth in claim 238, further comprising the acts of:

making a first product in response to the weighted image information; and

making a second product in response to the first product.

--476. A process as set forth in claim 241, further comprising the act of making a motion control product in response to the scaled weighted image information.

--477. A process as set forth in claim 241, further comprising the acts of:

making a computer aided design product in response to the process set forth in claim 241; and

making a second product in response to the computer aided design product.

--478. A process as set forth in claim 241, further comprising the acts of:

making a first product in response to the scaled weighted image information;

making a second product in response to the first product; and

making a third product in response to the second product.

--479. A process as set forth in claim 244, further comprising the act of making a positioned product.

--480. A process as set forth in claim 244, further comprising the acts of:

making a first product in response to the process set forth in claim 244; and

making a second product in response to the first product.

--481. A process as set forth in claim 249, further comprising the act of making a position control product in response to the process set forth in claim 249.

--482. A process as set forth in claim 249, further comprising the acts of:

making a computer aided design product; and

making a second product in response to the computer aided design product.

--483. A process as set forth in claim 249, further comprising the acts of:

making a first product in response to the process set forth in claim 249;

making a second product in response to the first product; and

making a third product in response to the second product.

--484. A process as set forth in claim 252, further comprising the act of making a signal product in response to the scaled weighted image information.

--485. A process as set forth in claim 252, further comprising the acts of:
making a first product; and
making a second product in response to the first product.

--486. A process as set forth in claim 255, further comprising the act of making a disk product.

506 I44 --487. A process as set forth in claim 255, further comprising the acts of:
making a design product in response to the 64-sample blocks of scaled weighted image information; and
making a second product in response to the design product.

H5 --488. A process as set forth in claim 255, further comprising the acts of:
making a first product;
making a second product in response to the first product; and
making a third product in response to the second product.

--489. A process as set forth in claim 258, further comprising the act of making a data compressed product in response to the process set forth in claim 258.

506 I45 --490. A process as set forth in claim 258, further comprising the acts of:
making a computer aided design product; and
making a second product in response to the computer aided design product.

--491. A process as set forth in claim 258, further comprising the acts of:
making a first product in response to the scaled weighted image information; and
making a second product in response to the first product.

--492. A process as set forth in claim 261, further comprising the act of making an oil product in response to the scaled weighted image information.

--493. A process as set forth in claim 261, further comprising the acts of:
making a display product in response to the process set forth in claim 261; and
making a second product in response to the display product.

--494. A process as set forth in claim 261, further comprising the acts of:
making a first product in response to the scaled weighted image information;
making a second product in response to the first product; and
making a third product in response to the second product.

--495. A process as set forth in claim 264, further comprising the act of making a building product.

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--496. A process as set forth in claim 264, further comprising the acts of:
making a design product in response to the weighted image information; and
making a second product in response to the design product.

--497. A process as set forth in claim 264, further comprising the acts of:
making a first product in response to the process set forth in claim 264; and
making a second product in response to the first product.

--498. A process as set forth in claim 267, further comprising the act of making a vehicle product in response to the process set forth in claim 267.

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--499. A process as set forth in claim 267, further comprising the acts of:
making a first product in response to the process set forth in claim 267;
making a second product in response to the first product; and
making a third product in response to the second product.

--500. A process as set forth in claim 270, further comprising the act of making a manufactured product in response to the scaled weighted image information.

--501. A process as set forth in claim 270, further comprising the acts of:
making a display product in response to the process set forth in claim 270; and
making a second product in response to the display product.

--502. A process as set forth in claim 270, further comprising the acts of:
making a first product, and
making a second product in response to the first product.

--503. A process as set forth in claim 273, further comprising the act of making a communication product.

--504. A process as set forth in claim 273, further comprising the acts of:
making a design product in response to the 64-sample blocks of scaled weighted information; and
making a second product in response to the design product.

--505. A process as set forth in claim 273, further comprising the acts of:
making a first product;
making a second product in response to the first product; and
making a third product in response to the second product.

--506. A process as set forth in claim 276, further comprising the act of making a communicated product in response to the process set forth in claim 276.

--507. A process as set forth in claim 276, further comprising the acts of:
making a first product in response to the scaled weighted image information; and
making a second product in response to the first product.

--508. A process as set forth in claim 279, further comprising the act of making a machined product in response to the 64-sample blocks of scaled weighted image information.

--509. A process as set forth in claim 279, further comprising the acts of:

making a display product in response to the process set forth in claim 279; and

making a second product in response to the display product.

--510. A process as set forth in claim 279, further comprising the acts of:

making a first product in response to the 64-sample blocks of scaled weighted image information;

making a second product in response to the first product; and

making a third product in response to the second product.